Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 x .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .035” X .035” DATE: 9/9/21**

**MFG: SILICONIX–LINEAR SYS. THICKNESS .009” P/N: SD5000**

**DG 10.1.2**

#### Rev B, 7/1